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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,938	07/13/2000	Kenji Shimazaki	32809	3985

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PEARNE & GORDON LLP
526 SUPERIOR AVENUE EAST
SUITE 1200
CLEVELAND, OH 44114-1484

EXAMINER	
BARAN, MARY C	
ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/615,938	SHIMAZAKI ET AL.	
	Examiner	Art Unit	
	Mary Kate B Baran	2857	

-- Th MAILING DATE of this communication appears on th cover sheet with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 January 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Respons to Amendm nt

1. This action is responsive to the Amendment filed 21 January 2003. Claims 1-8 are pending.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The proposed drawing correction was received on 21 January 2003. These corrections are approved by the Examiner. Corrected drawings are required in reply to this Office Action.

Specification

4. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finman (U.S. Patent No. 5,117,377) in view of Burch et al. (Pattern-Independent Current Estimation for Reliability Analysis of CMOS Circuits) (hereinafter Burch).

Referring to claim 1, Finman teaches analyzing electromagnetic interference which develops in an LSI (see Finman, column 1 lines 7-12), comprising a correction step of correcting the amplitude of a signal in each node (see Finman, column 5 lines 3-8), an addition step of adding the signals of all nodes together within a period of time corresponding to one cycle, provided that the thus-corrected signal appears at the time the signal arrives at the node (see Finman, column 5 lines 6-16), and a frequency analysis step of analyzing the frequency of the signal, calculated in the addition step (see Finman, column 6 lines 64-68). The examiner interprets the term "generic analyzer" as disclosed in Finman to mean the same as the claimed term "frequency analyzer" (see Finman, column 12 lines 29-34). Finman does not teach generating a current waveform, and calculating the current, which has been prepared for each change in each node, in accordance with the probability of variation in each node.

Burch teaches providing a current waveform for each node (see Burch, page 2 lines 7-9), and calculating the current in accordance with the probability of change in each node (see Burch, page 3 lines 2-5).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings of Burch, because calculating

the current based on the probability of change would have allowed the skilled artisan to determine the worst case current waveform (see Burch, page 1 lines 26-28).

Referring to clam 2, Finman further teaches correcting the amplitude of a signal in each node (see Finman, column 5 lines 3-8), but does not teach, a current estimation waveform, or monitoring the change in each node in accordance with a probability of variation and a distribution with respect to time.

Burch teaches a current estimation waveform (see Burch, page 2 lines 7-9), and monitoring the change in each node in accordance with a probability of variation (see Burch, page 3 lines 22-31) and a distribution with respect to time (see Burch, page 4 lines 7-10).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings Burch because monitoring the change in each node in accordance with a probability of variation and a time distribution would have allowed the skilled artisan to derive an accurate current waveform (see Burch, page 4 lines 16-17).

Referring to claims 3 and 4, Finman teaches all the features of the claimed invention except for each node having a plurality of signal transmission paths, and each of the current waveforms is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrive time.

Burch further teaches each node having a plurality of signal transmission paths (see Burch, page 2 lines 22-23), and each of the current waveforms is calculated in consideration of a case where each of the paths has a unique probability of change (see Burch, page 3 lines 22-31) and signal arrive time (see Burch, page 4 lines 7-10).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Finman to include the teachings of Burch, because calculating current with respect to a unique probability of change would have allowed the skilled artisan to derive an accurate current waveform (see Burch, page 4 lines 16-17).

6. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamaki et al. (U.S. Patent No. 5,784,285) (hereinafter Tamaki) in view of Burch et al. (Pattern-Independent Current Estimation for Reliability Analysis of CMOS Circuits) (hereinafter Burch).

Referring to claims 5 and 7, Tamaki teaches analyzing electromagnetic interference which develops in an LSI (see Tamaki, column 1 lines 5-9), comprising a waveform formation step forming a waveform (see Tamaki, column 4 lines 34-38) which has been prepared as if the waveform randomly arises within a plurality of predetermined cycles (see Tamaki, column 4 lines 17-22) adding the thus prepared waveforms to thereby derive a new waveform (see Tamaki, column 4 lines 16-28), and analyzing the frequency of the waveform, thereby determining a noise characteristic of EMI (see Tamaki, column 5 lines 1-20). Tamaki does not teach calculating the current,

which has been prepared for each change in each node, in accordance with the probability of change in each node and a time at which a signal arrives at each node.

Burch teaches calculating the current in accordance with the probability of change in each node (see Burch, page 3 lines 22-31) and a time at which a signal arrives at each node (see Burch, page 4 lines 7-10).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tamaki to include the teachings of Burch, because calculating the current based on the probability of change would have allowed the skilled artisan to determine the worst case current waveform (see Burch, page 1 lines 26-28).

Referring to claims 6 and 8, as noted above Tamaki teaches all the features of the claimed invention except that each node has a plurality of paths and a current is calculated in consideration of a case where each of the paths has a unique probability of change and signal arrival time.

Burch further discloses a method wherein each node has a plurality of paths (see Burch, page 2 lines 22-23) and a current is calculated in consideration of a case where each of the paths has a unique probability of change (see Burch, page 3 lines 22-31) and signal arrival time (see Burch, page 4 lines 7-10).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Tamaki to include the teachings of Burch, because calculating current with respect to a unique probability of change would have allowed the skilled artisan to derive an accurate current waveform (see Burch, page 4 lines 16-17).

Respons to Arguments

7. Applicant's arguments with respect to claims 1, 3 and 5-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Uchino et al. teaches a power estimation method for an integrated circuit using probability calculations.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B Baran whose telephone number is (703) 305-4474. The examiner can normally be reached on Monday - Friday from 8:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S Hoff can be reached on (703) 308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

MKB
April 2, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800